

In the Claims

The status of claims in the case is as follows:

We claim:

- 1 1. [Currently amended] A decoupling capacitor,
2 comprising:

3 a fixed resistance in series with said capacitor, said
4 capacitor formed by a polysilicon layer and a diffusion
5 layer, said fixed resistance formed by contacts
6 connecting said polysilicon layer to a first voltage
7 level buss and said diffusion layer to a second voltage
8 level buss said capacitor connected between said first
9 and second voltage level busses such that majority
10 carriers accumulate at a surface of a substrate
11 underneath a gate oxide layer without forming an
12 inversion layer; and

13 said contacts being of location and capacity for
14 protecting surrounding circuits in the event there is a
15 defect shorting said busses together by limiting defect
16 current while allowing said capacitor to function at a
17 frequency sufficiently high to suppress noise on said
18 first and second busses to a value which achieves bus
19 stability.

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1 2. [Previously presented] The decoupling capacitor of
2 claim 1, further comprising:

3 said contacts including a first set of contacts to a
4 first voltage and a second set of contacts to a second
5 voltage;

6 a defect leakage current limiting path including said
7 first set and said second sets of contacts separated by
8 a distance optimized to cause a defect shorting said
9 polysilicon layer to said substrate to force defect
10 current to travel from said first set of contacts
11 through a section of the substrate, then to the
12 polysilicon through the defect, and then along the rest
13 of the polysilicon layer to said second set of
14 contacts.

1 3. [Original] The decoupling capacitor of claim 2,
2 further comprising:

3 said first set of contacts and said second set of
4 contacts determined in number and location to provide
5 preselected minimum and maximum resistance values
6 between said first and second sets of contacts, said
7 minimum resistance value for achieving a preselected
8 maximum leakage current through any defect site in said

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9 polysilicon layer, and said maximum resistance value
10 for achieving a preselected overall decoupling RC
11 factor sufficient for a minimum RC network bandwidth.

1 4. [Original] The decoupling capacitor of claim 3,
2 further comprising providing said first and second sets of
3 contacts in sufficient number to effectively achieve total
4 contact resistance less than 10% of combined sheet
5 resistance of said diffusion and polysilicon layers across a
6 distance separating said first and second sets of contacts.

1 5. [Original] The decoupling capacitor of claim 2,
2 further comprising providing N pairs of contacts in said
3 sets of contacts and placing said first and second sets of
4 contacts separated by a distance K sufficient to achieve a
5 leakage limiting resistance of R and a bandwidth limiting
6 resistance of $R/2$.

1 6. [Original] The decoupling capacitor of claim 2,
2 further comprising providing a technology-dependent number
3 of contacts selected in number sufficient to achieve total
4 contact resistance less than 10% of combined sheet
5 resistance of said diffusion and polysilicon layers across a
6 distance separating said first and second sets of contacts.

1 7. [Withdrawn] A method for determining the number and
2 position of contacts in a decoupling capacitor including a
3 polysilicon layer and a diffusion layer, comprising:

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4 determining a maximum allowable defect current I for
5 IDDQ testing of said capacitor;

6 determining a minimum sheet resistance R to achieve
7 said defect current I ;

8 determining minimum distance K between first and second
9 sets of said contacts to achieve said minimum sheet
10 resistance R ;

11 determining number of said contacts N in said sets of
12 contacts to provide sufficiently low contact resistance
13 to assure said minimum sheet resistance R dominates
14 total resistance between said first and second sets of
15 contacts; and

16 providing in said decoupling capacitor contact sites of
17 sufficient area to accommodate N said contacts with
18 said first and second sets of said contacts separated
19 by at least distance K .

1 8. [Withdrawn] A program storage device readable by a
2 machine, tangibly embodying a program of instructions
3 executable by a machine to perform method steps for
4 determining the number and location of contacts in a
5 decoupling capacitor including a polysilicon layer and a
6 diffusion layer, said method comprising:

7 determining a maximum allowable defect current I for

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8 IDDQ testing of said capacitor;

9 determining a minimum sheet resistance R to achieve
10 said defect current I;

11 determining minimum distance K between first and second
12 sets of said contacts to achieve said minimum sheet
13 resistance R;

14 determining number of said contacts N in said sets of
15 contacts to provide sufficiently low contact resistance
16 to assure said minimum sheet resistance R dominates
17 total resistance between said first and second sets of
18 contacts; and

19 defining in said decoupling capacitor contact sites of
20 sufficient area to accommodate N said contacts with
21 said first and second sets of said contacts separated
22 by at least distance K.

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